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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,279	11/28/2001	Lothar Risch	L&L-I0178	4049

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,279	RISCH ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *21-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Receipt is acknowledged of the request under 35 U.S.C. 119(a)-(d), claiming priority from German Patent Application No. 199 24 571.1 filed May 28, 1999 however no original papers have been received and none of record in the file.

Continued Prosecution Application

The request filed on November 28, 2001 for a Continued Prosecution Application (CPA) under 35 U.S. C. 120 based on parent Application No. PCT/ DE00/01714 is acceptable and a CPA has been established. An action on the CPA follows.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filed February 15, 2002.

The references on PTO 1499 submitted on 2/15/2002 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

The initialed PTO 1-449 has been made of record and placed in the file along with instructions to the contract employees to mail a copy of the same along with the instant Office Action.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-20, are drawn to a method of fabricating a double gated MOSFET, classified in class 438, subclass 200 +.

II. Claims 21-25, are drawn to a double gate MOSFET, classified in class 257, subclass 123.

Inventions Group I (claims 1-20) and Group II (claims 21-25) are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case that the product as claimed can be made by another and materially different process namely instead of using the silicon substrate disclosed in the method claims other substrates like GaAs or other compound substrates can be used.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Markus Nolss on May 13 and 14, 2002 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-20

Affirmation of this election must be made by applicant in replying to this Office action.

Claim 21-25 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

Drawings

The drawings are objected to by the drafts person for reasons stated in the enclosed PTO- 948. Applicants' are reminded that under the new rules (see 37 CFR 1.85 (a)) drawings corrections cannot be held in abeyance and failing to file corrected drawings may result in abandonment of the application.

The disclosure is objected to because of the following informalities:

The specification page 10 line 25 recites " SIO" which must be replaced by "SOI".

Page 12 line 6" overgrown" must be replaced by " covered"

Appropriate correction is required.

Claim Objections

Claim 10 line 2 " selectively acting" should be changed to "selectively etching".

Claim Rejections - 35 USC § 112

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "spacer layer " in claim 1 is used by the claim to mean " separation/filler" while the accepted meaning is "sidewall spacer".

It is suggested that Applicants' use the term " separation" instead of the recited "spacer".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-2 and 4-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,365,465, herein after Chang).

With respect to claim 1, Chang discloses a method of fabricating a double gate MOSFET, including the steps of :

Providing a substrate having a silicon substrate layer (Fig. 1 A # 4, col. 4 lines 5-6); a first insulation layer disposed on the silicon substrate layer (Fig. 1 A # 3, col. 4 line 7); a first spacer layer disposed on the first insulation layer (Fig. 1 A #11); and a semiconductor layer disposed on the first spacer layer (fig. 1 A # 5): patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET (fig. 1 A #5, channel between s/d 9); depositing a second spacer layer on the semiconductor layer and the first spacer layer (fig. 3 A # 2); patterning the first and second spacer layers such that the semiconductor layer structure remains substantially completely embedded in the first and second spacer layers (Fig. 3A # 16 remains embedded within 2 and 6); depositing a second insulation layer on the structure formed of the first and second spacer layers (fig. 3A # 7): vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them: during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case; filling the depressions with electrically conductive material (fig. 3 C # 17), forming a contact hole in the second insulation layer (Fig. 2Y # 11); selectively removing the first and second spacer layers through the contact hole made in the second insulation layer (fig. 1 D); applying a third insulation layers on inner walls of a region of removed spacer layers

and on surfaces of the semiconductor layer structure (figs. 20 to 2Q) and introducing a further electrically conductive material into the region of the removed spacer layers. (2Y # 12).

It is noted that figs. 1A-1D, 2A-2BB and 3A-D all describe different embodiments, however as Chan itself describes in col. 6 lines 25-40 and 55-58 the steps of the embodiments describes in figs. 1-3 are interchangeably used.

With respect to claim 2, wherein the substrate structure is formed by applying the first insulation layer, the first spacer layer, and the semiconductor layer one after another. (See claim1 above. It is noted that current case law is , "As a matter of fact selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhaus, 154 F.2d 690, 69 USPQ330 (CCPA 1946, therefore without a showing of criticality or unexpected results the recited order of steps is prima facie obvious).

With respect to claim 4, wherein the forming the substrate includes the steps of : Providing the silicon substrate functioning as a first semiconductor substrate (fig. 1A # 4); applying the first insulation layer on the first semiconductor substrate (Fig. 1 A # 3, col. 4 line 7); providing a second semiconductor substrate (Fig. 1 a # 12); applying the first spacer layer on the second semiconductor substrate (fig. 1A # 11); connecting the first and second semiconductor substrates to one another using a wafer bonding process between the insulation layer and the first spacer layer(Figs. 2A to 2C, col. 4 lines 46-61) and reducing a thickness of the second semiconductor substrate resulting in the semiconductor layer (col. 4 lines 58-60, boron etch).

With respect to claim 5, wherein the first and second spacer layers are formed from silicon nitride (fig. 2 F layers # 2 & 7).

With respect to claim 6, wherein the second insulating layer is planarized after being deposited.(fig. 2G and col. 6 lines 64-66).

With respect to claim 7, wherein the step of selectively removing the first and second spacer layers through the contact hole made in the second insulation layer.(fig. 2G).

With respect to claims 8 and 13, wherein the electrically conductive material is formed from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide. (col. 6 lines 15-18).

With respect to claims 9 and 14, wherein the doped polycrystalline silicon is formed by Chemical Vapor phase deposition and a doping is performed during deposition. (col. 4 lines 27-29).

With respect to claim 10, the method comprises " using a selective acting (sic. Etching) , wet-chemical etching step for removing the first and second spacer layers.(col. 6 lines 1-5).

With respect to claim 11, the method comprises applying the third insulation layers using a thermal oxidation process. (col. 6 line 10).

With respect to claim 12, wherein the step of producing a relatively thin oxide layer on the surface of the semiconductor layer structure and producing a relatively thick oxide layer on the inner walls of the region of the removed spacer layers. (figs. 2C and 2 T , col. 4 lines 47-49 and col. 6 lines 9-14).

With respect to claim 15, wherein an oxide layer is applied as the first insulation layer (fig. 1 A).

With respect to claim 16, wherein a silicon layer is applied as the semiconductor layer(col. 6 line 15-17).

With respect to claim 17, wherein an oxide is deposited as the second insulation layer. (fig. 2G).

With respect to claim 18, wherein an oxide layer is applied as the third insulation layer.(fig. 2G).

With respect to claim 19, wherein arsenic atoms are used in the doping process. (col. 7 line 43)

With respect to claim 20, wherein phosphorous atoms are used in the doping process.(col. 7 line 44).

B. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,365,465, herein after Chan) as applied to claims 1-2 above, and further in view of Shimizu (U.S. Patent No. 5,753,541, herein after Shimizu).

With respect to claim 3, wherein the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

Chang does not specifically describe the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

However, Shimizu, a patent from the same filed of endeavor, describes in col. 5 lines 33-38 describes the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam to make the substrate a semi conductive layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include Shimizu's laser annealing step(i.e. recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam to make the substrate a semi conductive layer) in Chang's method so that further processing steps can use lower temperature than conventional methods wherein polycrystalline material is used. (Shimizu col. 3 lines 59-63).

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7722.

Steven H. Rao

Patent Examiner

July 29, 2002.

OLIK CHAUDHURI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER